EUROPRAXICE-IC SERVICE

ENABLE FOR LOW COST ASIC FOR R&D AND PRODUCT DEVELOPMENT

AMIT KHANNA

EPIXFAB TRAINING
27TH SEP, ECOC 2015
WHAT IS EUROPRACTICE?

Europractice is a service. Offering access to

- Exists since 1989 funded by the EC
- Professional and state-of-the-art EDA tools for IC/MEMS/PHOT/FPGA design at affordable cost at 650 European academia
- Professional and state-of-the-art technologies for IC/MEMS/PHOT prototyping at affordable cost at 650 European academia and users from around the world
- Companies use MPW prototyping and volume production at cost
EUROPEAN INSTITUTIONS USING EUROPRACTICE

- More than 650 institutions
  - ~ 530 universities
  - ~ 120 research institutes
- In 44 countries close to Europe
- Support contracts for design tools
- Common design infrastructure
  - Ideal basis for collaborative research projects
- Although it is an EC-funded project
  - 85% turnover is from end users!
  - Contributed to stability, long lifetime
EUROPRACTICE IC SERVICE

Current contract with the EC until mid 2020

Universities and R/D
- CAD tools for European univ only
- Libraries
- Technical support
- MPW Prototyping
- Packaging

> 650 European Universities
+ research labs

Companies
- Libraries
- Technical support
- MPW Prototyping
- Volume production
- Packaging & Test & Operations

CAD vendors
Cadence
Mentor-Graphics
Synopsys
...

Library vendors
ARM
Faraday
...

Foundries
Ams, IHP, imec,
GlobalFoundries
Memscap, OnSemi
UMC, TSMC, XFAB

Assembly houses
ASE
HCM

Test houses
ASE
Microtest
EUROPRAXICE IC SERVICE

**Universities and R/D**
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**Companies**
- Libraries
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~ 500 companies and non-European universities including 250 fabless companies in Europe

- Foundries: Ams, IHP, imec, GlobalFoundries, Memsca, OnSemi, UMC, TSMC, XFAB
- Assembly houses: ASE, HCM
- Test houses: ASE, Microtest

No CAD vendors: Cadence, Mentor-Graphics, Synopsys, ...

Library vendors: ARM, Faraday, ...

EUROPRAXICE
EUROPRACTICE DESIGN TOOL PORTFOLIO CAPABILITIES

3D-IC
Photonics layout & verification
PCB design
Package analysis
Thermal analysis
DFM and yield optimisation
Interconnect analysis
SiP
SoC
Sensors - image, pressure, fluidic, ...
MEMS / microfluidic design
RF design
Design for testability
High level synthesis
Design verification
“App” development on Virtual prototypes
Application specific processors
Hardware software co-design
Embedded processors
Design reuse – IP blocks
Mixed-signal design
Digital synthesis from HDL
Transistors
Layout
Process and device modelling

• European Universities and Research Institutes have diverse training and research needs
• This needs to be reflected in the breadth of the design tool portfolio
• Tools are not restricted to EUROPRACTICE processes or geometries
• Non-commercial use only
Foundries and IC Technologies

GlobalFoundries (Germany + Singapore)
- 55nm CMOS Low Power
- 40nm CMOS Low Power
- 28nm Super Low Power/High Performance Power

IHP (Germany)
- IHP SGB25V 0.25µ SiGe:C
- IHP SGB25VGOD 0.25µ SiGe:C
- IHP SG25H1 0.25µ SiGe:C
- IHP SG25H3P 0.25µ complementary SiGe:C
- IHP SG25H3 0.25µ SiGe:C
- IHP SG25H4 0.25µ SiGe:C
- IHP SG13G2 SiGe:C Bipolar/Analog
- IHP SG13S SiGe:C Bipolar/Analog/CMOS
- IHP SG13C SiGe:C CMOS 7M/MIM

XFAB (Germany)
- 0.18µ CMOS XH018 eFlash HV
- 0.18µ CMOS XT018 SOI HV

ON Semi (Belgium + USA)
- 0.7µ CMOS A/D 2M
- 0.5µ CMOS A/D 3M
- 0.35µ CMOS A/D 5M
- 0.7µ CMOS A/D I2T100
- 0.7µ CMOS A/D I2T30
- 0.35µ CMOS A/D I3T80/50/25
- 0.5µ CMOS C5 EEPROM

Selection criteria
- Well-known foundry
- Partnership
- Flexible prototyping
- Small + medium volume

ams (Austria)
- 0.35µ CMOS A/D 4M
- 0.35µ SiGe BICMOS 4M
- 0.35µ CMOS 50V
- 0.35µ CMOS OPTO
- 0.18µ CMOS + HV

UMC (Taiwan)
- 0.18µ CMOS L/MMC/RF
- 0.13µ CMOS L/MMC/RF
- 90nm CMOS L/MMC/RF
- 65nm CMOS L/MMC/RF
- CIS : 0.18µ
- CIS : 0.11µ

TSMC (Taiwan)
- Cell libraries and design kits for UMC 0.18, 0.13µ, 0.11µ, 90nm & 65nm CMOS
- 0.18µ CMOS L/MS/RF + HV
- 0.13µ CMOS L/MS/RF
- 90nm CMOS L/MS/RF
- 65nm CMOS L/MS/RF
- 40nm CMOS L/MS/RF
- 28nm CMOS LP (SiON)
- 28nm CMOS HPL (HKMG)

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SILICON PHOTONICS, MEMS FOUNDRIES

PSV

WaveGuide
FiberCoupler
Si substrate

ISIPP25G+

PolyMUMP

SOI MUMP

MetalMUMP

PiezoMUMP

Si310-PH

SG25_PIC

ihp

Cellectix

leti

MEMSCAP

Si substrate

WaveGuide

Si3

SiO2

PolyMUMP

SOI MUMP

MetalMUMP

PiezoMUMP
MPW FOR PROTOTYPING

- Mask cost is shared between customers
- Wafer fabrication cost is shared between customers
- You pay as you use
- Many MPW runs scheduled in each technology

Packaged samples

YOUR Design

Design A

Design B

Design n

2015 General Europractice MPW runs Schedule and Prices

Accessible for universities, research institutes and companies

www.europractice-ic.com
PROTOTYPING AT AFFORDABLE COST

Prototype cost vs. launch flexibility.

- **Full Mask**: Size ~ 20x30 mm, Any time.
- **MLM**: Size ~ 10x15 mm, Any time.
- **MPW**: Size per sqmm, MPW schedule.
- **mini@sic**: Size per subblock, Selected runs from MPW schedule.

Source: TSMC.
### MINI@SIC on Selected MPW Runs

**Technology node** | **mask + prototype cost (euro)** | **MPW cost** | **mini@sic cost**
---|---|---|---
0.7 micron | 20,000 | 10 | 3,500
0.35 micron | 50,000 | 10 | 6,000
0.18 micron | 100,000 | 25 | 15,000 | 3,000
90nm | 550,000 | 16 | 50,000 | 3.75 | 15,000
65nm | 750,000 | 12 | 50,000 | 3.75 | 18,000
40nm | 1,200,000 | 9 | 65,000 | 3.5 | 22,000
**ISIPP25G+** | NA | 25 | 40,000 | 6.25 | 10,000
**SI310PH** | NA | 26 | 28,650 | 6.29 | 6,960

**Notes:**
- UMC 0.18u, UMC 0.13u, TSMC 0.18u
- UMC 90nm, UMC 65nm, TSMC 90nm
- TSMC 65nm
- TSMC 40nm
- Technology node
- Mask + prototype cost (euro)
- MPW cost
  - Area (mm²)
  - Cost (euro)
- Mini@sic cost
  - Area (mm²)
  - Cost (euro)
HISTORY OF TECHNOLOGY USAGE
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MEMS & SiPhoton... 0.8µ...0.5µ 0.35µ 0.25µ 0.18µ...0.1 5µ 0.13µ...0.1 1µ 90nm 65nm 40nm 28nm
DESIGNS PER TECHNOLOGY NODE - 2014

technology node and number of designs in 2014

- 0.13μ...0.11μ, 94
- 0.18μ...0.15μ, 155
- 0.35μ, 121
- 0.25μ, 47
- 0.8μ...0.5μ, 4
- 90nm, 14
- 65nm, 50
- 40nm, 1
- 28nm, 1
- MEMS & SiPhotonics, 48
DESIGNS PER COUNTRY

Number of IC and MtM designs prototyped on MPW runs through EUROPRACTICE
Europractice completed 545 designs using 10 technology nodes in 2014 (ASIC+PIC+MEMS)

Europractice brokers MPW runs in Photonics for IMEC, LETI, and IHP (Booth # 808)
PHOTONICS DESIGN SERVICE

Preparing to launch Photonics Design and IP Network

**IP-Block sale**

Different maturity levels and complexity

Black-box white box availability

Use per run tracking and black box replacement

**Design support service**

*Available in 2016!*
<table>
<thead>
<tr>
<th>Access Type</th>
<th>Availability</th>
<th>Technology</th>
<th>Price</th>
</tr>
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<tbody>
<tr>
<td>Black Box</td>
<td>Single run</td>
<td>Basic</td>
<td>M=0 M=1 M=2</td>
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<tr>
<td></td>
<td>multiple use/run</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Advanced</td>
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<tr>
<td></td>
<td>Unlimited use</td>
<td>Basic</td>
<td>M=0 M=1 M=2</td>
</tr>
<tr>
<td>White Box*</td>
<td>Unlimited use + portability support agreement</td>
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</tbody>
</table>

*Black box price is refunded on subsequent White box purchase
M=0, simulation only. M=1 silicon tested at least once, M=2 silicon tested on more than 2 runs
PHOTONICS PACKAGING

Launched in Feb 2015
Standardized packaging document
Standardized pricing

▷ Description of layout guidelines
▷ Packaged device performance characteristics
▷ Multiple passive device package options (single fiber, arrays, vertical and in-plane coupling for grating couplers, edge coupler packaging)
▷ Standardized layout for active components – bond pads, DC pads, electro-optical bandwidth considerations
▷ Mechanical stability, thermal considerations (peltiers) etc.
ACCESS PROCESS AND TAT

Stage1: Get PDK

Sign NDA/DKLA (obtain from Europractice website)

Send the scanned copy back to us

In a week Username/Password for PDK download is supplied

Stage2: Identify MPW

Register to an upcoming run for fabrication

Stage3: Iterate design until DRC clear

For a new user on ISIPP25G+ (1-2 months)

Stage4: Fabrication – 4 to 6 months

Stage5: Characterization and analysis - 2 months

Overall 6-9 month cycle from DRC clean design1 to design2 submission.
BOOTH 808

TALK 1
28\textsuperscript{TH} SEP, 12:30
EUROPEAN PHOTONIC INTEGRATION FORUM
FERIA DE MUESTRAS, JOAQUIN RODRIGO ROOM
WWW.EPIF2015.ORG

TALK 2
30\textsuperscript{TH} SEP, 13:15-13:45
ECOSYSTEM FOR CMOS PHOTONICS LOW VOLUME PRODUCTION
MARKET FOCUS EXHIBITION HALL

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